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<i>DB=USPT; PLUR=YES; OP=OR</i>			
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<u>L7</u>	L1 and (scoreboard\$3 or table) near9 (valid\$8 or invalidat\$4 or invalid\$5)	47	<u>L7</u>
<u>L6</u>	L5 and l2	72	<u>L6</u>
<u>L5</u>	L4 or l3	19610	<u>L5</u>
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Search Results - Record(s) 1 through 20 of 44 returned.

☐ 1. Document ID: US 6658559 B1

L14: Entry 1 of 44

File: USPT

Dec 2, 2003

US-PAT-NO: 6658559

DOCUMENT-IDENTIFIER: US 6658559 B1

TITLE: Method and apparatus for advancing load operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Attachments	Claims	KWIC	Draw De
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☐ 2. Document ID: US 6640313 B1

L14: Entry 2 of 44

File: USPT

Oct 28, 2003

US-PAT-NO: 6640313

DOCUMENT-IDENTIFIER: US 6640313 B1

TITLE: Microprocessor with high-reliability operating mode

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Attachments	Claims	KWIC	Draw De
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☐ 3. Document ID: US 6615366 B1

L14: Entry 3 of 44

File: USPT

Sep 2, 2003

US-PAT-NO: 6615366

DOCUMENT-IDENTIFIER: US 6615366 B1

TITLE: Microprocessor with dual execution core operable in high reliability mode

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Attachments	Claims	KWIC	Draw De
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☐ 4. Document ID: US 6598156 B1

L14: Entry 4 of 44

File: USPT

Jul 22, 2003

US-PAT-NO: 6598156

DOCUMENT-IDENTIFIER: US 6598156 B1

TITLE: Mechanism for handling failing load check instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 5. Document ID: US 6526499 B2

L14: Entry 5 of 44

File: USPT

Feb 25, 2003

US-PAT-NO: 6526499

DOCUMENT-IDENTIFIER: US 6526499 B2

TITLE: Method and apparatus for load buffers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 6. Document ID: US 6425072 B1

L14: Entry 6 of 44

File: USPT

Jul 23, 2002

US-PAT-NO: 6425072

DOCUMENT-IDENTIFIER: US 6425072 B1

TITLE: System for implementing a register free-list by using swap bit to select first or second register tag in retire queue

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 7. Document ID: US 6412067 B1

L14: Entry 7 of 44

File: USPT

Jun 25, 2002

US-PAT-NO: 6412067

DOCUMENT-IDENTIFIER: US 6412067 B1

TITLE: Backing out of a processor architectural state

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 8. Document ID: US 6412064 B1

L14: Entry 8 of 44

File: USPT

Jun 25, 2002

US-PAT-NO: 6412064

DOCUMENT-IDENTIFIER: US 6412064 B1

**** See image for Certificate of Correction ****

TITLE: System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 9. Document ID: US 6393556 B1

L14: Entry 9 of 44

File: USPT

May 21, 2002

US-PAT-NO: 6393556

DOCUMENT-IDENTIFIER: US 6393556 B1

**** See image for Certificate of Correction ****

TITLE: Apparatus and method to change processor privilege without pipeline flush

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 10. Document ID: US 6360309 B1

L14: Entry 10 of 44

File: USPT

Mar 19, 2002

US-PAT-NO: 6360309

DOCUMENT-IDENTIFIER: US 6360309 B1

TITLE: System and method for assigning tags to control instruction processing in a superscalar processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 11. Document ID: US 6256729 B1

L14: Entry 11 of 44

File: USPT

Jul 3, 2001

US-PAT-NO: 6256729

DOCUMENT-IDENTIFIER: US 6256729 B1

TITLE: Method and apparatus for resolving multiple branches

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 12. Document ID: US 6223278 B1

L14: Entry 12 of 44

File: USPT

Apr 24, 2001

US-PAT-NO: 6223278

DOCUMENT-IDENTIFIER: US 6223278 B1

TITLE: Method and apparatus for floating point (FP) status word handling in an out-of-order (OOO) Processor Pipeline

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 13. Document ID: US 6216215 B1

L14: Entry 13 of 44

File: USPT

Apr 10, 2001

US-PAT-NO: 6216215

DOCUMENT-IDENTIFIER: US 6216215 B1

**** See image for Certificate of Correction ****

TITLE: Method and apparatus for senior loads

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 14. Document ID: US 6138231 A

L14: Entry 14 of 44

File: USPT

Oct 24, 2000

US-PAT-NO: 6138231

DOCUMENT-IDENTIFIER: US 6138231 A

TITLE: System and method for register renaming

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 15. Document ID: US 6131157 A

L14: Entry 15 of 44

File: USPT

Oct 10, 2000

US-PAT-NO: 6131157

DOCUMENT-IDENTIFIER: US 6131157 A

TITLE: System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 16. Document ID: US 6108771 A

L14: Entry 16 of 44

File: USPT

Aug 22, 2000

US-PAT-NO: 6108771

DOCUMENT-IDENTIFIER: US 6108771 A

TITLE: Register renaming with a pool of physical registers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 17. Document ID: US 6092176 A

L14: Entry 17 of 44

File: USPT

Jul 18, 2000

US-PAT-NO: 6092176
DOCUMENT-IDENTIFIER: US 6092176 A

TITLE: System and method for assigning tags to control instruction processing in a superscalar processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 18. Document ID: US 6088790 A

L14: Entry 18 of 44

File: USPT

Jul 11, 2000

US-PAT-NO: 6088790
DOCUMENT-IDENTIFIER: US 6088790 A

TITLE: Using a table to track and locate the latest copy of an operand

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 19. Document ID: US 6000044 A

L14: Entry 19 of 44

File: USPT

Dec 7, 1999

US-PAT-NO: 6000044
DOCUMENT-IDENTIFIER: US 6000044 A

TITLE: Apparatus for randomly sampling instructions in a processor pipeline

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 20. Document ID: US 5974538 A

L14: Entry 20 of 44

File: USPT

Oct 26, 1999

US-PAT-NO: 5974538
DOCUMENT-IDENTIFIER: US 5974538 A

TITLE: Method and apparatus for annotating operands in a computer system with source instruction identifiers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 21. Document ID: US 5966530 A

L14: Entry 21 of 44

File: USPT

Oct 12, 1999

US-PAT-NO: 5966530

DOCUMENT-IDENTIFIER: US 5966530 A

TITLE: Structure and method for instruction boundary machine state restoration

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 22. Document ID: US 5896542 A

L14: Entry 22 of 44

File: USPT

Apr 20, 1999

US-PAT-NO: 5896542

DOCUMENT-IDENTIFIER: US 5896542 A

TITLE: System and method for assigning tags to control instruction processing in a superscalar processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 23. Document ID: US 5892963 A

L14: Entry 23 of 44

File: USPT

Apr 6, 1999

US-PAT-NO: 5892963

DOCUMENT-IDENTIFIER: US 5892963 A

TITLE: System and method for assigning tags to instructions to control instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 24. Document ID: US 5859998 A

L14: Entry 24 of 44

File: USPT

Jan 12, 1999

US-PAT-NO: 5859998

DOCUMENT-IDENTIFIER: US 5859998 A

TITLE: Hierarchical microcode implementation of floating point instructions for a microprocessor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Drawings
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☐ 25. Document ID: US 5848288 A

L14: Entry 25 of 44

File: USPT

Dec 8, 1998

US-PAT-NO: 5848288

DOCUMENT-IDENTIFIER: US 5848288 A

TITLE: Method and apparatus for accommodating different issue width implementations of VLIW architectures

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Drawings
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☐ 26. Document ID: US 5828873 A

L14: Entry 26 of 44

File: USPT

Oct 27, 1998

US-PAT-NO: 5828873

DOCUMENT-IDENTIFIER: US 5828873 A

TITLE: Assembly queue for a floating point unit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Drawings
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☐ 27. Document ID: US 5826055 A

L14: Entry 27 of 44

File: USPT

Oct 20, 1998

US-PAT-NO: 5826055

DOCUMENT-IDENTIFIER: US 5826055 A

TITLE: System and method for retiring instructions in a superscalar microprocessor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Drawings
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☐ 28. Document ID: US 5805853 A

L14: Entry 28 of 44

File: USPT

Sep 8, 1998

US-PAT-NO: 5805853

DOCUMENT-IDENTIFIER: US 5805853 A

**** See image for Certificate of Correction ****

TITLE: Superscalar microprocessor including flag operand renaming and forwarding

h e b b cg b cc e

apparatus

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 29. Document ID: US 5768556 A

L14: Entry 29 of 44

File: USPT

Jun 16, 1998

US-PAT-NO: 5768556

DOCUMENT-IDENTIFIER: US 5768556 A

TITLE: Method and apparatus for identifying dependencies within a register

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 30. Document ID: US 5764938 A

L14: Entry 30 of 44

File: USPT

Jun 9, 1998

US-PAT-NO: 5764938

DOCUMENT-IDENTIFIER: US 5764938 A

TITLE: Resynchronization of a superscalar processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 31. Document ID: US 5751985 A

L14: Entry 31 of 44

File: USPT

May 12, 1998

US-PAT-NO: 5751985

DOCUMENT-IDENTIFIER: US 5751985 A

TITLE: Processor structure and method for tracking instruction status to maintain precise state

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 32. Document ID: US 5673426 A

L14: Entry 32 of 44

File: USPT

Sep 30, 1997

US-PAT-NO: 5673426

DOCUMENT-IDENTIFIER: US 5673426 A

TITLE: Processor structure and method for tracking floating-point exceptions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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h e b b c g b c c e

☐ 33. Document ID: US 5673408 A

L14: Entry 33 of 44

File: USPT

Sep 30, 1997

US-PAT-NO: 5673408

DOCUMENT-IDENTIFIER: US 5673408 A

TITLE: Processor structure and method for renamable trap-stack

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 34. Document ID: US 5659721 A

L14: Entry 34 of 44

File: USPT

Aug 19, 1997

US-PAT-NO: 5659721

DOCUMENT-IDENTIFIER: US 5659721 A

TITLE: Processor structure and method for checkpointing instructions to maintain precise state

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 35. Document ID: US 5655115 A

L14: Entry 35 of 44

File: USPT

Aug 5, 1997

US-PAT-NO: 5655115

DOCUMENT-IDENTIFIER: US 5655115 A

TITLE: Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 36. Document ID: US 5651124 A

L14: Entry 36 of 44

File: USPT

Jul 22, 1997

US-PAT-NO: 5651124

DOCUMENT-IDENTIFIER: US 5651124 A

TITLE: Processor structure and method for aggressively scheduling long latency instructions including load/store instructions while maintaining precise state

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 37. Document ID: US 5649225 A

L14: Entry 37 of 44

File: USPT

Jul 15, 1997

US-PAT-NO: 5649225

DOCUMENT-IDENTIFIER: US 5649225 A

**** See image for Certificate of Correction ****

TITLE: Resynchronization of a superscalar processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 38. Document ID: US 5649136 A

L14: Entry 38 of 44

File: USPT

Jul 15, 1997

US-PAT-NO: 5649136

DOCUMENT-IDENTIFIER: US 5649136 A

TITLE: Processor structure and method for maintaining and restoring precise state at any instruction boundary

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 39. Document ID: US 5644742 A

L14: Entry 39 of 44

File: USPT

Jul 1, 1997

US-PAT-NO: 5644742

DOCUMENT-IDENTIFIER: US 5644742 A

TITLE: Processor structure and method for a time-out checkpoint

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 40. Document ID: US 5632023 A

L14: Entry 40 of 44

File: USPT

May 20, 1997

US-PAT-NO: 5632023

DOCUMENT-IDENTIFIER: US 5632023 A

**** See image for Certificate of Correction ****

TITLE: Superscalar microprocessor including flag operand renaming and forwarding apparatus

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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